Design and Analysis of Power and Variability Aware Digital Summing Circuit

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***Abstract*— Due to aggressive scaling and process imperfection in sub-45 nm technology node V_t (threshold voltage) shift is more pronounced causing large variations in circuit response. Therefore, this paper presents the analyses of various popular 1-bit digital summing circuits in light of PVT (process, voltage and temperature) variations to verify their functionality and robustness. The investigation is carried with ±3ó process parameters and ±10% V_{DD} (supply voltage) variation by applying Gaussian distribution and Monte Carlo analysis at 22 nm technology node on HSPICE environment. Design guidelines are derived to select the most suitable topology for the design features required. Transmission Gate (TG)-based digital summing circuit is found to be the most robust against PVT variations. Hence, a TG-based digital summing circuit is implemented using carbon nanotube field effect transistor (CNFET). This implementation offers tighter spread in propagation delay (3×), power dissipation (1.14×) and EDP (energy delay product) (1.1×) at nominal voltage of V_{DD} = 0.95V compared to MOSFET-based (TG – topology) digital summing circuit implying its robustness against PVT variations.**

***Index Terms*—Carbon nanotube field effect transistor (CNFET), transmission gate (TG), random dopant fluctuation (RDF), line edge roughness (LER), energy delay product (EDP).**

I. Introduction

As CMOS reaching the scaling limits, the need for alternative technologies are necessary. Nanotechnology-based fabrication is expected to offer the extra density and potential performance to take electronic circuits the next step. Several nanoscale electronic devices are demonstrated in the recent past by researchers, some of the most promising being carbon nanotube based field effect transistor (CNFET). The digital summing circuit is one of the most important and critical building block of any Digital System. Many computation intensive applications such as multimedia processing and digital communication can now be realized in hardware to either speed up the operation or reduce the power consumption. The essence of the digital computing lies in the full adder design. Hence, the optimization of the full adder cell in terms of speed and power dissipation is not only important but also its robustness against PVT (process, voltage and temperature) variations is essential. Some comparison among full adder circuits are found in the in the literature [1]–[3]. None of these previous works was targeted for variability analysis. This paper investigates, for the first time to the best of our knowledge, various topologies of (including recently proposed) 1-bit full adder cell against PVT variations at 22 nm technology node. It also proposes CNFET - based 1-bit digital summing circuit (hereafter called TG(CNT)) for the most robust CMOS adder topology namely TG-based full adder cell (hereafter called TG(MOS)). It demonstrates that the TG(CNT) outperforms TG(MOS) not only in terms of EDP but also in terms of robustness. The remainder of this paper is organized as follows. Impact of RDF (random dopant fluctuation) is briefly discussed in Section II. Various topologies of 1-bit digital summing circuits are briefly analysed in Section III. Section IV presents brief introduction of CNFET structure, which is used for the proposed design. Simulation results and comparisons between TG(MOS) and TG(CNT) are explained in Section V. Section VI concludes this article.

II. Impact of Random Dopant Fluctuation

Due to aggressive device scaling, there are several design challenges for nanoscaled circuit design. Intrinsic parameter fluctuations like random dopant fluctuation (RDF), line edge roughness (LER) and variation in oxide thickness fluctuate threshold voltage (V_t). The intra-die V_t variation due to RDF results in deviation of design goal. The standard deviation of the V_t fluctuation due to RDF depends on the manufacturing process, doping profile and the transistor sizing and is given by [4]

$$\sigma_{V_t} = \frac{q t_{ox}}{\varepsilon_{ox}} \sqrt{\frac{N_{SUB} W_{dm}}{3LW}} \qquad (1)$$

where W_{dm} is the maximum gate depletion width, ε_{ox} is oxide relative permittivity, t_{ox} is the oxide thickness, q is the electronic charge, N_{SUB} is the substrate doping concentration, L (W) is the channel length (width). Variation in V_t due to RDF is 30 mV (15 mV) in subthreshold (linear) region for a sub-100 nm device with W = 50 nm, L = 100 nm, t_{ox} = 30 Å and N_{SUB} = 8.6×10^{17} cm^{-3} [5]. Propagation delay (t_p), power dissipation (P) and EDP (energy delay product) are important design metrics of digital circuit. The distributions of these metrics are even more problematic than their absolute values because meeting the design specification with variations in them is difficult for a designer. The spread in these design metrics are estimated based on Central Limit Theorem [6]. As per the Central Limit Theorem, the distribution of a random variable (say, Y) which is the summation of a large number of independent random variables (say, X_1, ..., X_n) can be assumed to be Normal with mean (μ) and the standard deviation (σ) given by

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$$\mu_Y = \sum_{i=1}^{n} \mu_{Xi} \text{ and } \sigma_Y^2 = \sum_{i=1}^{n} \sigma_{Xi}^2. \quad (2)$$

If all the variables are identically distributed (i.e. all with equal mean μ_X and standard deviation σ_X) we further obtain

$$\mu_Y = N\mu_X \text{ and } \sigma_Y = \sqrt{N}\,\sigma_X$$
$$\Rightarrow \frac{\sigma_Y}{\mu_Y} = \frac{1}{\sqrt{N}} \frac{\sigma_X}{\mu_X}. \quad (3)$$

From (3), it is observed that, the spread (standard deviation (σ)/mean(μ)) of the variable Y is less than the spread in the variable X and the spread of Y reduces as more number of variables is added together. Monte Carlo simulations are carried out to investigate and measure the impact of PVT variations on the t_p, P and EDP in the sections to come.

III. Analysis of 1-bit Digital Summing Circuits

This section presents analysis of the most popular topologies of 1-bit digital summing circuits including recently proposed circuits. The circuit diagram of static CMOS 1-bit full adder cell is shown in Fig. 1 [7]. The circuit is described by the following Boolean equations [8]

$$\overline{CARRY} = \overline{C(B+A)+BA} \quad (4)$$

$$SUM = CBA + (C+B+A)\overline{CARRY}$$
$$= CBA + (C+B+A)\overline{(C(B+A)+BA)}. \quad (5)$$

The main drawback of static CMOS circuits is the existence of the PMOS block, which is slow because of the low mobility of its holes (therefore, the PMOS devices are upsized (2-3×) to attain the desired performance. The input capacitance of a static CMOS gate is large because each input is connected to the gate of at least a PMOS and an NMOS device. Another static CMOS full adder analyzed is Mirror full adder shown in Fig. 2 [7], [8]. This topology is implemented just by connecting directly the series PMOS transistors to the supply voltage, since when A = B = 0, the series connected PMOS transistors are connected to V_{DD} to raise the input of both the inverters for sum (S) and carry (Co). The Transmission gate (TG) based 1-bit full adder [8] called TG(MOS) shown in Fig. 3, is a high-speed low-power full adder, but if cascaded in series, its propagation delay increases which may be unacceptable in case of long chain of full adders. This problem is mitigated in TGdrivcap full adder [8] shown in Fig. 4.

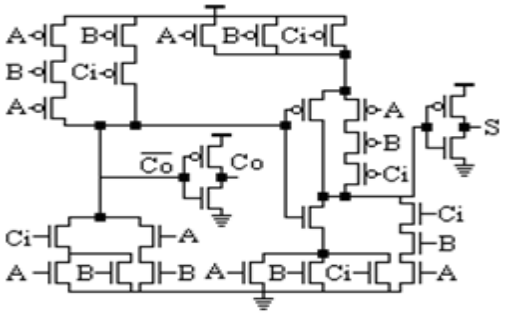

Figure 1. Static CMOS 1-bit full adder

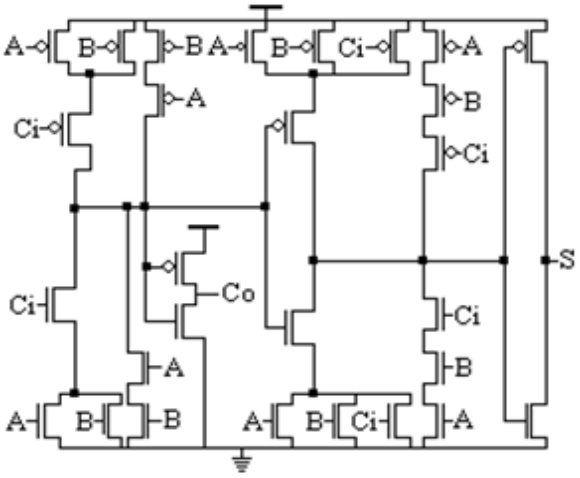

Figure 2. Mirror full adder

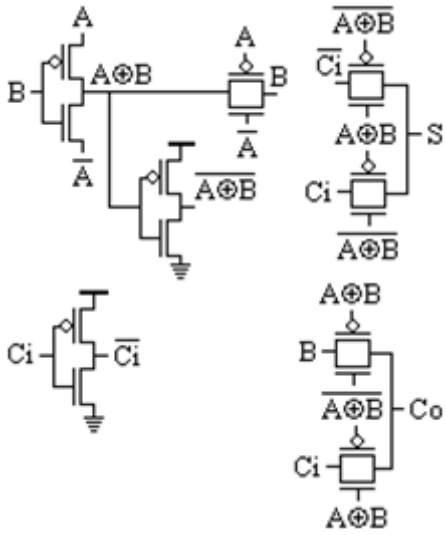

Figure 3. TG(MOS) version of 1-bit full adder

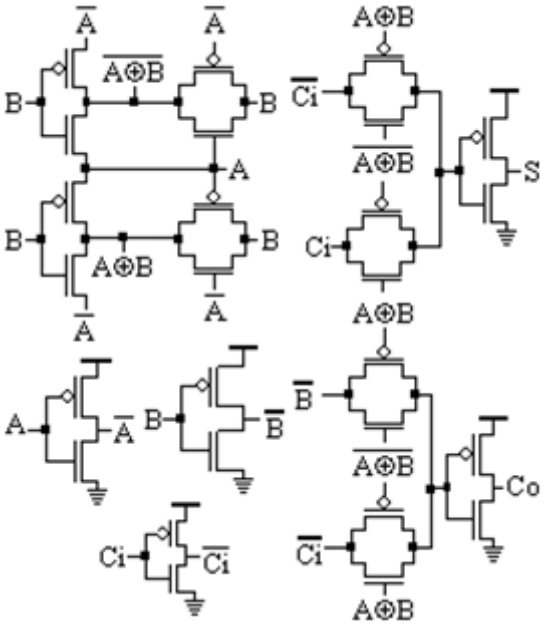

Figure 4. TGdrivcap

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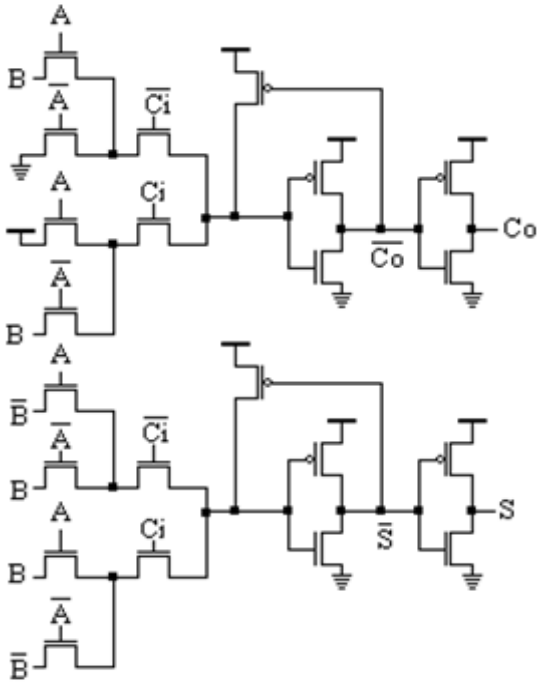

Figure 5. Leap full adder

The LEAP (Lean Integration with Pass-Transistor) adder shown in Fig. 5 is an attempt to clarify the possibilities of top-down pass-transistor design [9]. Due to worst case $2\times V_t$ drop in transmission of input A and B at the input of first two inverters two weak PMOS keeper transistors are used. This topology functions correctly at V_{DD} = 1 V with V_t = 0.4 V [9], but does not functions correctly at lower voltages. The hybrid full adder shown in Fig. 6 is based on XOR–XNOR circuit that generates XOR and XNOR full swing outputs simultaneously. Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application [10]. The Complementary Pass-transistor Logic (CPL) [11] full adder considered for the analysis in this paper is shown in Fig. 7.

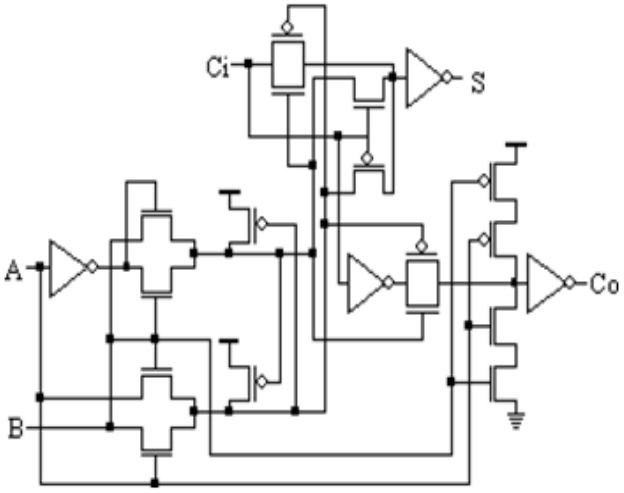

Figure 6. Hybrid full adder

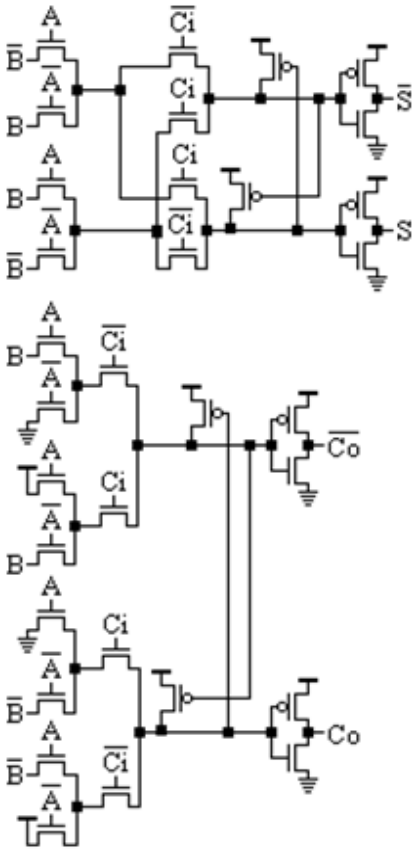

Figure 7. CPL version of 1-bit full adder

The CPL has topology with differential inputs and it is implemented with NMOS pass-transistors. The cross-coupled PMOS transistors for SUM (S) and CARRY (Co) outputs are used as level restorer to reduce the short-circuit power dissipation. This topology provides high-speed and full-swing operation. It has good driving capability due to the presence of output static inverters and the fast differential stage of cross-coupled PMOS transistors. However, due to the presence of a lot of internal nodes and static inverters, there is large power dissipation. Other recently proposed 1-bit full adders such as 8T, 10T full adder [12] shown in Fig. 8 and 9, 12T full adder [13] shown in Fig. 10, 14T and CLRCL (complementary and level restoring carry logic) full adder [14] shown in Fig. 11 and 12 are analyzed in this work. The results of the analyses are not reported here because these full adders function well up to 50 kHz at higher technology nodes, whereas these analyses are carried out at 100 MHz at V_{DD} ranging from 1 V down to 0.7 V at 22 nm technology node. The dynamic CMOS logic style provides a high speed of operation because the logic is constructed with only high mobility NMOS transistors. In addition, due to the absence of the PMOS transistors, the input capacitance is also low, thus enhancing the speed of operation. However, it has several inherent drawbacks such as charge sharing and high clock load. Albeit it has higher switching activity, it has lower noise immunity; it consumes a larger portion of the power in driving the clock lines. Moreover, dynamic logic style is more susceptible to leakage. Due to these reasons, full adders with dynamic logic style are not considered for analysis in this paper.

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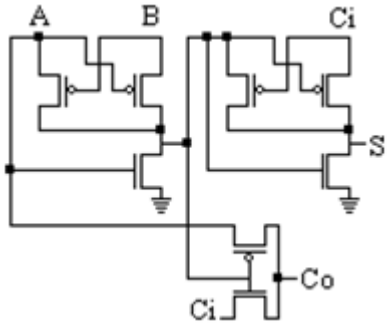

Figure 8. 8T full adder

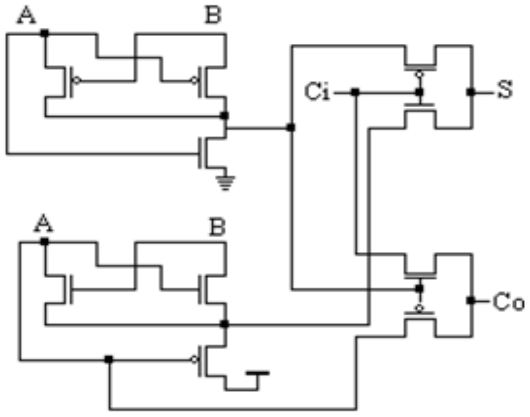

Figure 9. 10T full adder

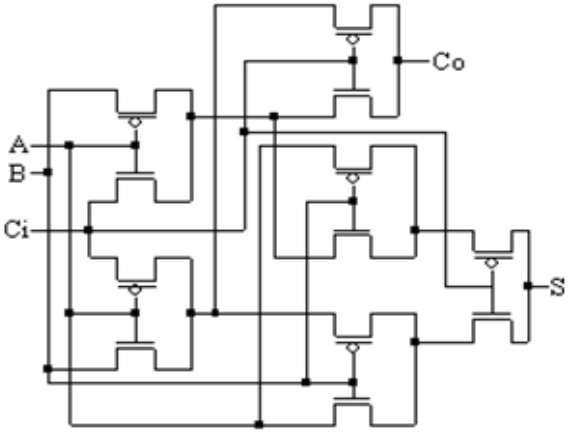

Figure 10. 12T full adder

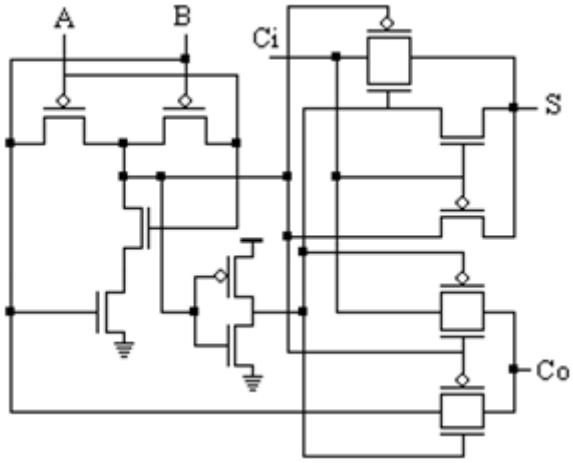

Figure 11. 14T full adder

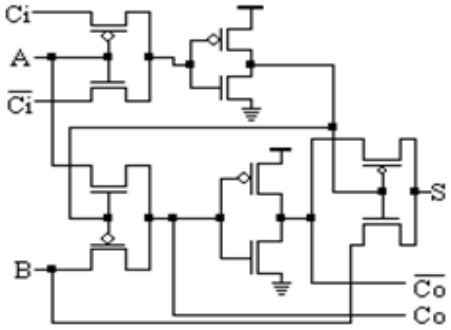

Figure 12. CLRCL full adder

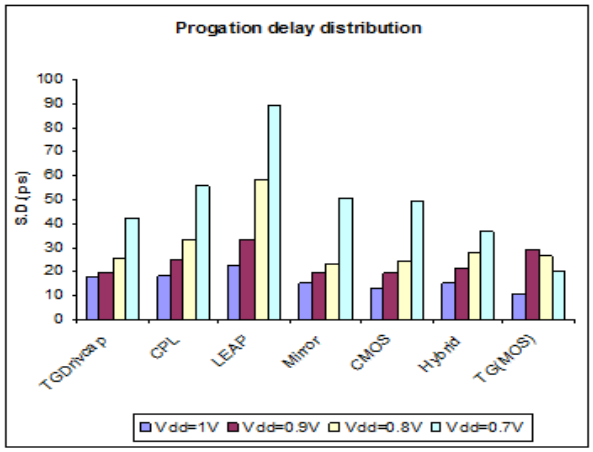

Figure 13. Propagation delay distribution

Since the overall speed of an n-bit full adder relies on the delay of final carry output, it makes sense to estimate propagation delay (t_p) considering delay between Ci (carry in) and Co (carryout). Thus, t_p is estimated as the time interval between the time the input signal (Ci) takes to reach 50% of its logic swing and the time the output signal (Co) takes to reach the same value. The power consumption (P) is estimated by taking the average power P_{avg}) delivered by V_{DD}.

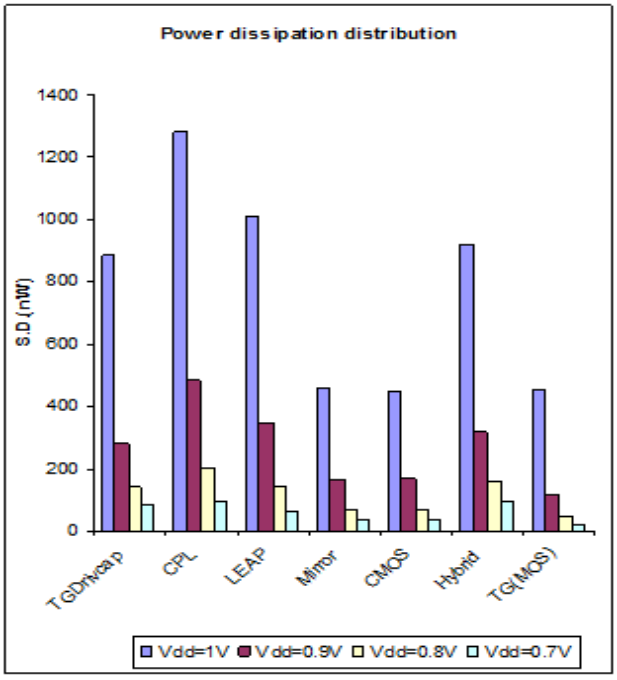

Figure 14. Power dissipation distribution

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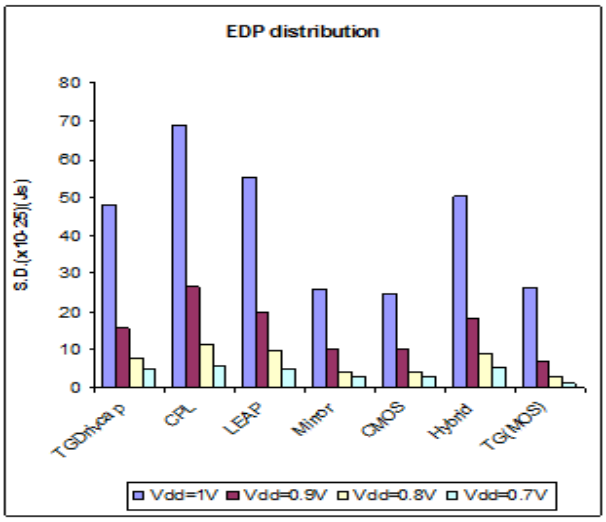

Figure 15. EDP distribution

Reducing EDP (energy delay product) is a good direction for optimizing VLSI design for portable use since ED product reflects the battery consumption (E) for completing a job in a certain time (D). The EDP is estimated as the product of $(t_p)^2$ with average dissipated power, P (i.e., P_{avg}). However, due to lack of space measured values of t_p, P and EDP of all full adders are not reported here, rather their dispersions are presented, since dispersion in these metrics are severe at highly scaled technology node such as 22 nm. As the S.D. (standard deviation) is a measure of dispersion that states numerically the extent to which individual observations vary on the average, it is used as a measure of variation in full adder design metrics such as t_p (propagation delay), P (power dissipation) and EDP (energy delay product). Dispersion analyses of full adder topologies of Fig. 1–7 are presented in Fig. 13, 14 and 15. It is observed from these figures that TG(MOS) is the best among all these MOSFET full adder topologies in terms of dispersion of these vital parameters at all considered supply voltages. This is attributed to the fact that the parallel devices in TG average out the impact of PVT variations. Therefore, it is selected for comparison with proposed TG(CNT). Moreover, P and EDP of CPL, CMOS (representative of full adders with driving capability) and TG(MOS) (representative of full adder without driving capability) are plotted in Fig. 16 and 17. As mentioned earlier, due to the presence of many internal nodes and static inverters, there is large power dissipation in CPL. This is evident from Fig. 16, which shows average power dissipation of CPL CMOS and TG(MOS).

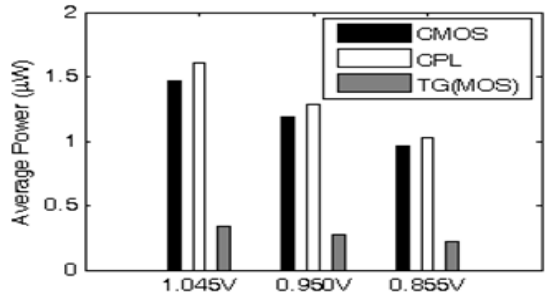

Figure16. Average power dissipation of MOSFET full adder topologies

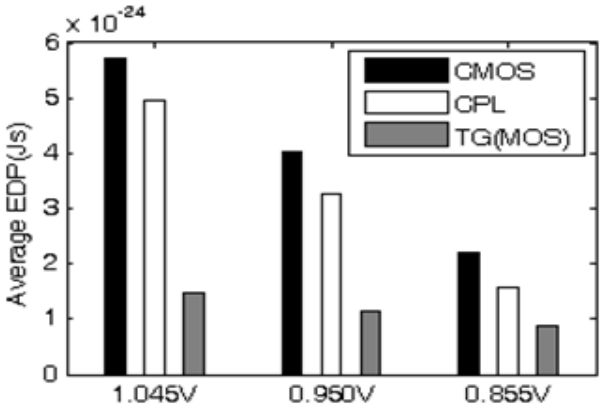

Figure 17. Average energy delay product of MOSFET full adder topologies

Thus, TG(MOS) full adder topology outperforms other two topologies in terms of average power dissipation. Fig. 17 shows average EDP of CPL, CMOS and TG(MOS) and exhibits superiority of TG(MOS) among these topologies.

IV. CNFET Structure and Its Characteristics

The cylindrical carbon nanotubes (CNTs) exhibit extraordinary strength and unique electrical properties. Their name is derived from their size, since the diameter of a nanotube is on the order of a few nanometres, while they can be up to 18 centimetres in length (as of 2010) [15]. CNT is categorized as single-walled carbon nanotube (SWCNT) as shown in Fig. 18(a) and multi-walled carbon nanotube (MWCNT) as shown in Fig. 18(b). Most SWCNTs have a diameter of close to 1 nm, with a tube length that can be many millions of times longer. The structure of a SWCNT can be conceptualized by wrapping a one-atom-thick layer of graphite called graphene into a flawless cylinder. One useful application of SWCNTs is in the development of CNFET. Production of the first logic gate using CNFET has recently become possible [16]. As variation in feature size and V_t is inherent to technology scaling, it is difficult to improve device performance by reducing the feature size of the devices beyond 45 nm technology generation. Hence, last few years witnessed a tremendous increase in nanotechnology research, especially the nanoelectronics. CNTs are the most studied material because of their unique mechanical and electronic properties. With ultralong (~1µm) mean free path for elastic scattering, a ballistic or near-ballistic transport can be obtained with the use of CNT under low voltage bias to achieve the ultimate device performance [17]–[20]. Its quasi-1-D structure provides better electrostatic control over the channel region. Ballistic transport operation and low I_{OFF} (off current) make the CNFET a suitable device for high performance and increased integration. The CNT acts as metal if $n_1 = n_2$ or $(n_1 – n_2)/3 = i$, where i is an integer. Otherwise, CNT works as semiconductor. The V_t of CNFET can be varied with CNT diameter (D_{CNT}). V_t of CNFET is approximated to the first order as the half band gap (V_t H" E_g/ 2q), which is an inverse function of diameter. The D_{CNT} and V_t of CNT are calculated using chirality vector (n_1, n_2) and V_π respectively as [21]

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$$D_{CNT} = \frac{a}{\pi}\sqrt{n_1^2 + n_2^2 + n_1 n_2} \quad (6)$$

$$V_t \approx \frac{E_g}{2q} = \frac{aV_\pi}{\sqrt{3} \times qD_{CNT}} \quad (7)$$

where E_g is energy gap, q = electronic charge, a = "3d = 2.49 Å is the lattice constant (where d H" 1.44 Å is the inter–carbon–atom distance) and V_π = 3.033 eV is the carbon π–to–π bond energy in the tight bonding model. In this work, CNFETs with chiral vector value (19, 0) are used. The D_{CNT} of the CNFET with chiral vector value (19, 0) is computed using (6) to be 1.5 nm. The V_t of the CNFET with chiral vector value of (19, 0) is computed using (7) to be 0.29 V.

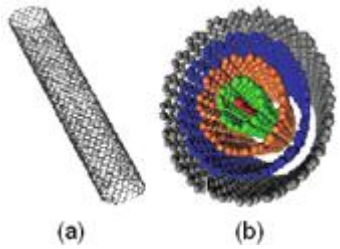

Figure 18. (a) SWCNT (Single-walled carbon nanotube), and (b) MWCNT (Muli-walled carbon nanotube)

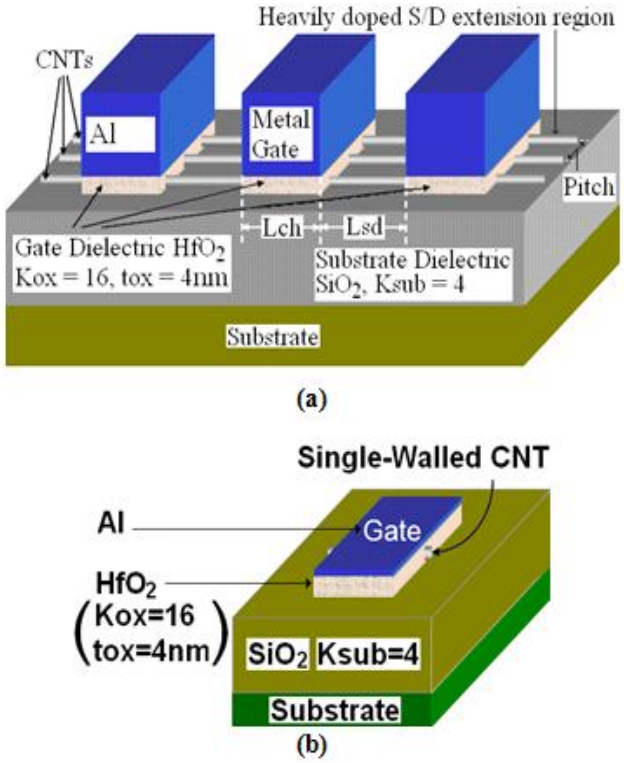

Figure 19. A typical CNFET structure with (a) multiple CNT and (b) single CNT (with high-*k* gate dielectric material HfO_2) [22], [23]

Compared to CMOS circuits, the CNFET circuit with one to ten CNTs per device is about two to ten times faster [22], [23]. A typical structure of a CNFET with multiple CNTs is illustrated in Fig. 19(a). Fig. 19(b) illustrates a CNFET structure with single CNT. CNTs are placed on substrate having dielectric constant of K_{sub} = 4. The channel region of CNTs is un-doped, and the other regions of CNTs are heavily doped. The tubes are separated by a high-k (Hi-k) material called hafnium (HfO_2) having dielectric constant of (K_{ox}) 16 and thickness (t_{ox}) of 4 nm. The effective width (Fig. 19(a)) of the multi-tubed CNFET (W_g) is defined as W_g = Pitch×(N_{CNT})+D_{CNT}, where Pitch is the distance between centre of two adjacent tubes, N_{CNT} is the number of tubes and D_{CNT} is the diameter of tube. Other important device and technology parameters related to CNFET are tabulated in Table I. The I-V characteristics of used CNFETs with chirality vector (19, 0) and minimum-sized square NMOS (22 nm × 22 nm) with zero bias threshold voltage, V_{tn0} = 0.68858 V are plotted in Fig. 20. P-type CNFET used in the proposed design has I-V characteristics with opposite polarity (not shown). The threshold voltages of N-CNFET are computed using (6) and (7) with chirality vector ranging from (7, 0) to (36, 0). First, the D_{CNT} is estimated substituting the value of the constant ð = 3.142, the value lattice constant a = 2.49 Å and the value of n_1 ranging from 7 to 36 keeping n_2 = 0. Next, the threshold voltage V_t is estimated substituting the value of a = 2.49 Å, the value of the carbon ð-to-ð bond energy $V_ð$ = 3.033 eV, the value of electronic charge $q = 1.6\times10^{-19}$ C and the estimated value of D_{CNT}. The estimated values of threshold voltages for each values of n_1 ranging from 7 to 36 are plotted in Fig. 21. The plot in Fig. 21 shows the V_ts of N-type CNFET with CNTs of different chirality vectors. For P-type CNFET, the V_t has an opposite polarity. The plot in Fig. 21 shows two end-points with V_t = 0.78857 V at n_1 = 7 and V_t = 0.153 V at n_1 = 36. Other important point in this plot is (19, 0.29) which indicates V_t = 0.29 V at n_1 = 19. This is the threshold voltage of CNFETs used in the proposed design.

TABLE I. DEVICE AND TECHNOLOGY PARAMETERS FOR CNFET

Parameter	Description	Value
L_{ch}	Physical channel length	22 nm
W_g	The width of metal gate (sub_pitch)	6.4 nm
t_{ox}	The thickness of high-k top gate dielectric material (planer gate).	4 nm
K_{ox}	Dielectric constant of high-K gate oxide	16
(n_1, n_2)	Chirality of the tube	(19, 0)
n_CNT	Number of tube per device	4

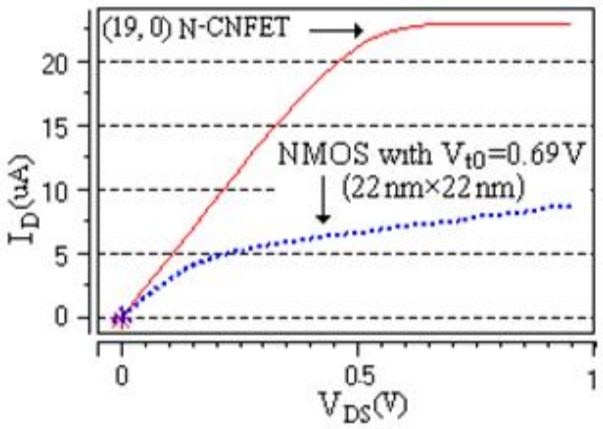

Figure 20. Comparison of I-V characteristics of NMOS and N-CNFET

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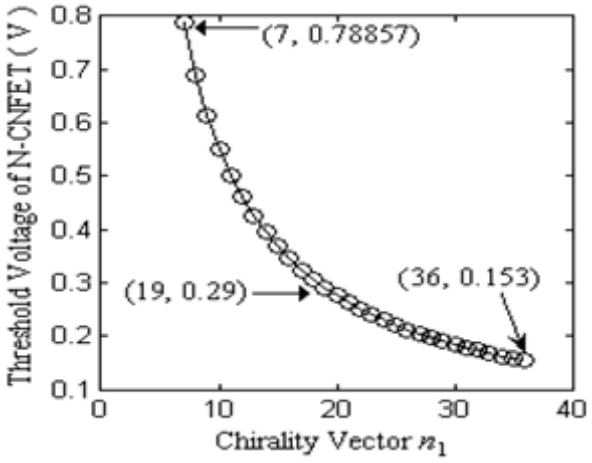

Figure 21. Threshold voltage (V_t) versus chirality vector (n_1)

V. Simulation results of Proposed CNFET-Based 1-Bit Digital Summing Circuit and Comparison

To simulate real environment, buffers are used for all inputs of the test circuit. A minimum output load of fan-out of four inverters (FO4) is used for power, delay and EDP measurements. The simulation test bench for the 1-bit full adder, which is circuit under test (CUT), is shown in Fig. 22. All the previous and following simulations are carried out using this simulation test bench. Analyses of full adders in Section III show that the TG-based 1-bit full adder topology exhibits immunity against PVT variations compared to other digital summing circuits. Therefore, in this paper CNFET-based 1-bit full adder cell of TG topology is designed, and its performance is assessed and compared with MOSFET version, i.e., TG(MOS). Fig. 23 shows the proposed design. Equations (4) and (5) are implemented by the proposed design as is done by its CMOS counterpart. The summation of two currents I_{Dn} and I_{Dp} flowing through NMOS and PMOS transistors of a transmission gate is primarily responsible for the lower value of variability in case of TG-based design. This averaging is impossible in case of other designs due to absence of parallel transistors. Variability of t_p is estimated as the standard deviation of delay divided by mean delay. The comparison of t_p distribution between TG(MOS) and TG(CNT) is reported in Table II and plotted in Fig. 24 for making comparison easier. The values normalized with respect to TG(CNT) are reported in bracket. It is observed from the Table II that the variability of t_p of TG(MOS) is wider than that of TG(CNT) at all supply voltages, particularly at nominal voltage of V_{DD} =0.950 V, it is 3× wider than that of TG(CNT).

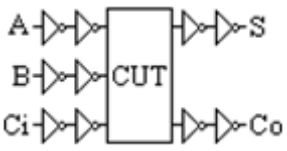

Figure 22. Simulation test bench

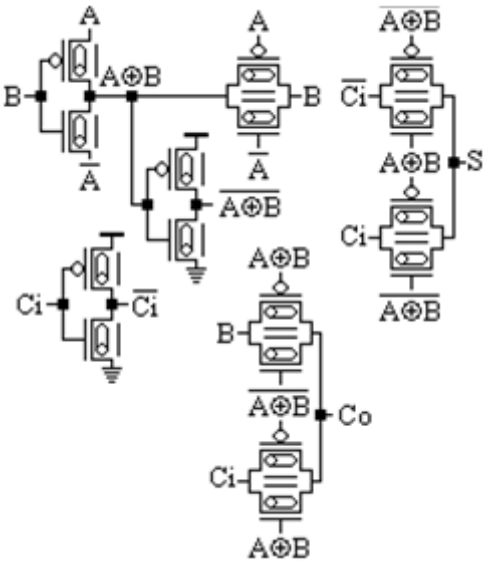

Figure 23. Proposed TG(CNT)

Table I. Variability of Propagation Delay

Full Adder Topology	(σ/μ) @ 1.045V	(σ/μ) @ 0 .950V	(σ/μ) @ 0.855V
TG(MOS)	0.003(10)	0.003(3)	0.010(14.3)
TG(CNT)	0.0003(1)	0.0010(1)	0.0007(1)

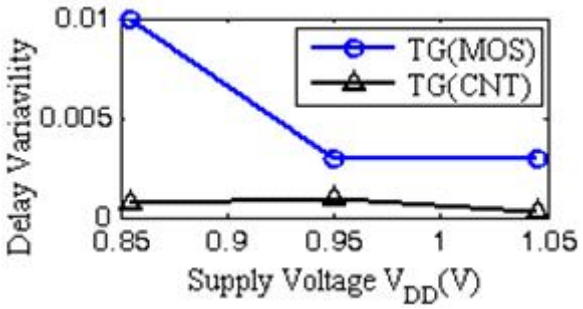

Figure 24. Propagation delay variation versus V_{DD} plot

This happens because a variation in the gate oxide thickness that strongly affects the drive current and capacitance of CMOS transistors has a negligible impact on the CNFET's operation. Hence, TG(CNT) is superior to TG(MOS) 1-bit full adder in terms of delay. It is needless to say that, TG(CNT) digital summing circuit will outperform the other full adder topologies analyzed earlier. The only drawback of TG(CNT) is its configuration, which is transmission gate based. With this configuration, the output is not isolated from the input, whereas the topologies such as static CMOS, Mirror, and CPL adder circuits isolate the output from the input and their driving capability is higher. As observed from Fig. 20, the drive current of CNFET is higher than that of a minimum-sized NMOS transistor. This is due to appropriate selection of chirality vector to estimate its V_t as shown in Fig. 21, which shows that the V_t of CNFET can be varied from 0.78857 V to 0.153 V with n_1 ranging from 7 to 36 keeping n_2 = 0. The V_t used for CNFET is much lower than that that of MOSFET. Of course, the drive current of CNFET used in TG(CNT) can further be enhanced by using more number of tubes. CNFETs with four tubes are used for increasing the driving capability of TG(CNT) digital summing circuit proposed in this paper.

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The comparison of power variation between TG(MOS) and TG(CNT) is reported in Table III. The values normalized with respect to TG(CNT) are reported in bracket. It is observed from the Table III, that the power dissipation variability of TG(MOS) is wider than that of TG(CNT) full adder circuit.

TABLE III. VARIABILITY OF POWER DISSIPATION

Full Adder Topology	(σ/μ) @ 1.045V	(σ/μ) @ 0 .950V	(σ/μ) @ 0.855V
TG(MOS)	0.005(1.25)	0.008(1.14)	0.010(1.43)
TG(CNT)	0.004(1)	0.007(1)	0.007(1)

The likely causes are attributed to the fact that the gate width in CNFET is not the effective channel width of the transistor. The channel width actually depends only on the tube diameter and the number of tubes under the gate. Hence, unlike MOSFET, variation of the conventional channel width does not affect the drive current. Only the CNT diameter has strong impact on its drive current, while other process parameter variations have very small impact. The impact of DIBL (drain-induced barrier lowering) or SCE (short-channel effect) is pronounced on drive current of MOSFET compared to that of CNFET. This is evident from the simulated result shown in Fig. 20, which shows that I_D of MOSFET increases almost linearly with V_{DS} after V_{DS} reaches V_{DSAT} (drain to source saturation voltage), whereas I_D (drain current) of CNFET remains almost constant even after V_{DS} exceeds V_{DSAT}. This feature exhibits immunity of CNFET against DIBL and SCE. Variability of EDP is estimated as the standard deviation of EDP divided by mean EDP. The comparison of EDP distribution between TG(MOS) and TG(CNT) is reported in Table IV. The values normalized with respect to TG(CNT) are reported in bracket and plotted in Fig. 25 for making the comparison easier. It is observed from the Table IV and Fig. 25, that the EDP variation of TG(MOS) is wider than that of TG(CNT) at all the considered supply voltages, and in particular, it is 1.1× wider at nominal voltage of V_{DD} = 0.950 V. This reflects the robustness of TG(CNT) full adder cell. Therefore, TG(CNT) full adder outperforms all the digital summing circuits (full adders) considered for analysis in this work.

TABLE IV. VARIABILITY OF EDP

Full Adder Topology	(σ/μ) @ 1.045V	(σ/μ) @ 0 .950V	(σ/μ) @ 0.855V
TG(MOS)	0.007(1)	0.011(1.1)	0.018(2.8)
TG(CNT)	0.007(1)	0.010(1)	0.007(1)

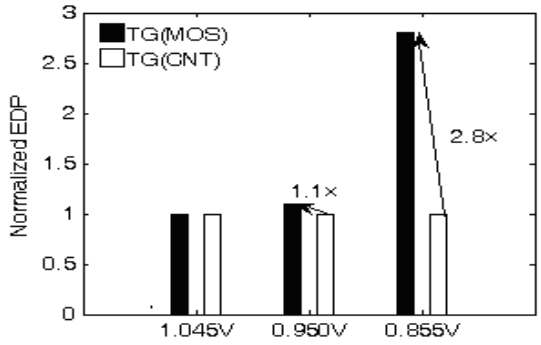

Figure 25. Comparison of EDP between TG(MOS) and TG(CNT)

VI. CONCLUSION

This paper analyzes the robustness of various digital summing circuits and proposes a CNFET version of the most robust MOSFET topology. It demonstrates that CNFET-based digital summing circuit is more robust against process and temperature variations compared to MOSFET digital summing circuits. It also demonstrates with simulation results that the proposed design performs well with supply voltage variation (±10% of V_{DD}) under appropriate loading conditions at 22 nm technology node. The proposed CNFET-based design will be an attractive choice to replace MOSFET version of digital summing circuit to achieve higher immunity against PVT variations.

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